Rayfes A. Mondal

311 W 5th St Unit 606
Austin, Texas 78701
512.850.5347
rayfes@siliconsoftware.com

PROFILE

Electrical engineer with **19+** years of specialized expertise in chip design, applications engineering, account management, and technical marketing. Highly analytical, creative problem solver with history of establishing and maintaining positive working relationships with diverse customers. Rapid learner energized by highly technical work in a fast-paced environment which includes top quality peers and cutting edge learning opportunities.

PROFESSIONAL EXPERIENCE

CADENCE DESIGN SYSTEMS, Austin TX 2010-Present
Principal Product Marketing Engineer

- Project management for IP deliveries involving schedule tracking and resource allocation.
- Manage pre-sales and post-sales customer support for DDR PHY IP.
- Org award for extraordinary achievements

DENALI SOFTWARE (acquired by Cadence), Austin TX 2007-2010
Senior Technical Marketing Engineer

- Launched new product offering of hardened PHY for DDR memory solutions by giving product demos, writing datasheets, strengthening relationships with partners, honing marketing messages and training our sales organization.
- Supported memory controller IP by assisting sales and providing market research.

ZENASIS TECHNOLOGIES, Austin TX (acquired by OpenSilicon) 2004-2007
Senior Applications Engineer

- Enhanced intranet to include resources such a global scripts repository, searchable group email archives along with creating numerous App Notes.
- Taught training to customers and new employees and created DAC demo.
- Assisted customers in optimizing their designs for timing, area, and leakage power.
- Worked closely with R&D and marketing on product road map and specifications.
- Grew sales by delivering value proposition to potential clients and performed tool evaluation demonstrating direct benefits on real customer designs.
- Successfully managed the company's largest million dollar account while developing relationships and driving sales with new accounts.

AUSTIN TECHNOLOGY CONSULTING, Austin, TX 2002-Present
Founder and President (mostly inactive due to Denali duties)

- Engineering consulting support for Silicon Software Solutions, an EDA tool distributor.

    - Assist sales efforts as a technical resource, presenter, and relationship manager.
    - Support multiple tools during pre-sales, evaluation, and post-sales as an applications engineer.
- Facilitated sales and development of flow and data management software (SAGE) with Thyme Technology, a small methodology consulting organization.
- Architected and implemented back-end database driven dynamic web projects for Nion Interactive, a fast growing web design and interactive advertising firm.
- Rescued Synopsys I2C DesignWare project by completing verification effort. Previous team spent six weeks trying to accomplish what I finished in seven days.

SYNOPSYS, Austin, TX 2000-2002
THE SILICON GROUP, Austin, TX (acquired by Synopsys) 1998-2000
Senior IC Design Engineer

- Acted as technical lead for creating a DesignWare I2C AMBA APB peripheral. Involved performing market research, writing functional spec, verification plan, and schedule, implementing verification plan, and coordinating team members. Design added to Synopsys DesignWare IP.
- Developed Vera testbenches for a datapath intensive design involving signal processing for a major defense contractor. First pass silicon success.
- Designed a re-usable DDR SDRAM memory controller for the Synopsys IP portfolio. Involved market research, writing the functional spec, developing micro-architecture, and the verilog RTL coding.
- Acted as project lead for developing a CRC block in NCL (asynchronous) logic for the Synopsys IP portfolio.
- Performed power analysis on a MIPS compatible core.
- Created a memory compiler to automatically characterize memory performance using SPICE to quickly explore potential design architectures.
- Fully developed an FPGA based design that incorporated a Low Pin Count bus interface, clean-sheet UART, and TIP interface used for testing Legacy Free PCs. Involved writing verilog RTL code, testbench, developer's manual and programming guide for a major microprocessor company. Assisted initial lab work.

INTERNATIONAL META SYSTEMS, Austin, TX 1998
Logic Design Engineer

- Modified the ALU of a high speed DSP to meet faster timing specs, performed static timing analysis, formal verification, and simulation.

STANDARD MICROSYSTEMS CORPORATION, Austin, TX 1996 to 1998
ASIC Design Engineer

- Verified the USB block within a PCI South Bridge through behavioral and gate level simulation and produced test vectors through the PLI interface
- Integrated a Synopsys PCI model into simulation environment.

ADVANCED MICRO DEVICES, Austin, TX 1994 to 1995
Embedded Processors Division, EE Co-op

- Simulated the embedded processor used to create world's smallest web server.
- Developed lab tests for pre-screening chips for alpha customers.

TECHNICAL EXPERTISE

Chip Design and Documentation:

Tech writing: func. specs, verif. plans, datasheets, char reports and user guides
Architecture, floorplanning, and HDL coding of designs for synthesis and reusability
Synthesis and verification of RTL HDL code along with constraint generation
Static Timing Analysis (STA) with Signal Integrity, along with Power Analysis
Physical placement and detailed routing
Standard cell library augmentation with tactical cells – layout generation, DRC/LVS, boundary checking, extraction, SPICE characterization, automated view creation
NCL logic design (asynchronous, clock-less, delay insensitive)

Tools: *Synopsys* Design/Phys Compiler, VCS+Vera, Formality, PrimeTime-SI, PowerMill *Magma* Mantle*, Cadence* Verilog-XL, First Encounter, Opus *Chrysalis* Design Verifier, *Novas* Debussy, *Xilinx* Alliance, *Orcad*, *Denali* PureView

Languages:

Verilog, VHDL, C, Java, awk, sed, perl, TCL, HTML, XML, PHP, SQL, assembly

FORMAL SPECIALIZED TRAINING

- *Synopsys*:Advanced Vera, Physical Compiler, Design Compiler, Primetime-SI, Formality, Design for Test (ATPG), Verilog Coding Styles for Synthesis, Chip Synthesis, Chip Architect
- Celoxica DK1 – Handel-C (C-based hardware modeling)

COMMUNITY SERVICE

- Director, HOA Board at the Plaza Lofts overseeing a $500k annual budget
- Volunteer Computer Lab Assistant, Hill Elementary School, Austin, TX
- Judge, Austin Area Science Fair, Austin, TX
- Volunteer, Salvation Army Christmas Gift Packages, Austin, TX
- Mentor, Electrical Engineering students, University of TX at Austin
- GRE Math Tutor for graduate school applicants, Austin, TX

EDUCATION

B.S. Electrical Engineering, University of Texas, Austin, TX 1996

- Honors Senior Project